Temporal Noise Suppression Method using Noise-Bandwidth Limitation for Pixel-Level Single-Slope ADC

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***Abstract*— This paper proposes a method for reducing temporal random noise (RN) in a pixel-level single-slope (SS) analog-to-digital converter (ADC) of a global-shutter (GS) CMOS image sensor (CIS). Pixel-level SS ADC is the ultimate scheme to improve image performances such as image quality, speed, noise, dynamic range, and power consumption compared to the column-level ADC. A temporal RN of the readout circuit represents flicker noise and thermal noise in the frequency domain. The noise-bandwidth limiting (nBWL) technique in the SS ADC circuit is a well-known method to limit the high-frequency response. By decreasing the -3dB cutoff frequency of the operational transconductance amplifier (OTA) for the comparator, the effective noise bandwidth is changed, and as a result a large portion of the thermal noise is filtered out. In order to achieve a low temporal noise global shutter imager, we have developed the pixel-wise ADC architecture with a 2-stacked structure including a large BWL capacitor. By finding an optimized size of the BWL capacitor to improve the RN performance, a precise circuit simulation and the related measurement were implemented. Because of the nBWL effect, the RN of the developed GS CIS with the BWL capacitor, approximately 100fF, has been reduced over 30% compared with the GS CIS without BWL capacitor. This noise reduction method is applied to our digital pixel sensor (DPS), which has a 4.95-μm pixel pitch and 2-megapixel (Mp) resolution, and the DPS has been successfully evaluated and demonstrated.**

Keywords—CMOS Image sensor, global shutter, pixel-level ADC, noise bandwidth limitation, temporal random noise, flicker noise, thermal noise, single-slope ADC

I. INTRODUCTION

Recently, the demands for the CMOS image sensor (CIS), especially a global shutter (GS) CIS, are increasing not only for mobile camera applications but also for machine vision image sensor applications such as an augmented reality (AR)/virtual reality (VR)/merged reality (MR), a security, and the automotive products. Until now, one of the main streams for CIS industry was a higher pixel resolution (larger than 200Mp) and a pixel shrinkage (less than 1.0 μm) based on the conventional column-parallel readout architecture [1-3]. In this case, however, some image degradation, such as dark shading, fixed-pattern noise (FPN), large power consumption, sensor noise, and so on, are still issued, and to solve the problems, we need next-generation readout architecture like as pixel-parallel readout scheme [4-6]. A single-slope (SS) analog-to-digital converter (ADC)-type readout scheme, which is mainly utilized for the consumer imaging devices, is excellent candidate for the pixel-level readout approach. Because of limitation of pixel area, only a very simple amplifier and ADC configuration can be implemented. The SS ADC, which compares the integration of the input with a reference level and measures the time the integrator takes to reach this reference level, is one of the simplest forms of integrating ADCs. In spite of the area advantage of SS ADC for pixel-level readout scheme, the ADC noise is basically degraded by the size shrinkage of the comparator, normally 20 times smaller than that of the conventional. To minimize ADC noise, the noise-bandwidth limiting (nBWL) technique is utilized to the developed digital pixel sensor (DPS) [7-8]. In general, nBWL method with column-parallel readout scheme used in a limited role to suppress the sensor noise including flicker and thermal noises, because of keeping the sensor operation speed. On the other hand, nBWL method with pixel-parallel readout scheme can be aggressively used for eliminating the noise components in high-frequency thermal noise region, because a longer A/D conversion time is secured by using global A/D conversion operation, not conventional row-by-row A/D conversion.

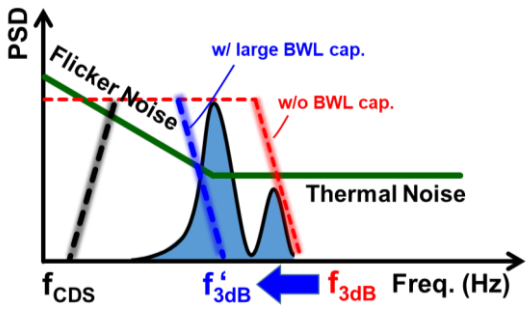


Figure 1. Conceptual noise power spectral density with/without nBWL technique.

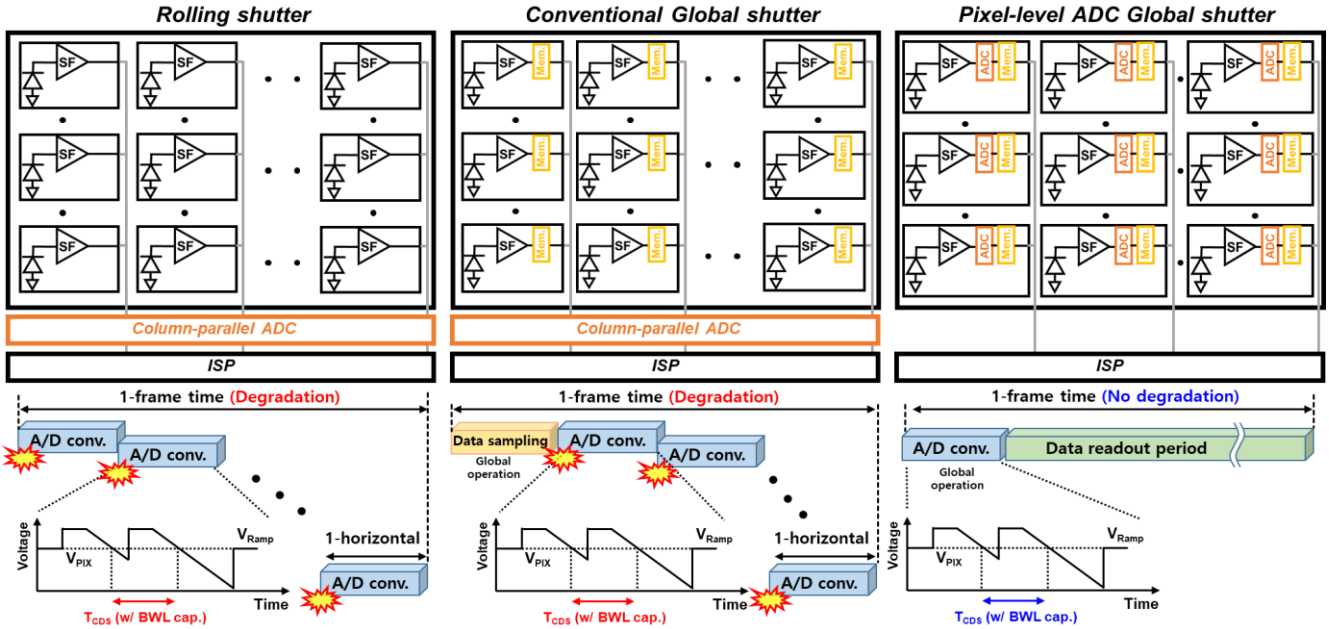
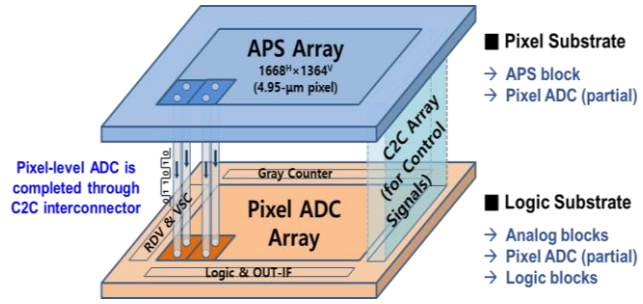


Figure 2. Sensor block diagrams with each simplified timing diagram for (a) Rolling shutter, (b) Conventional global shutter and (c) Pixel-level ADC global shutter architecture.

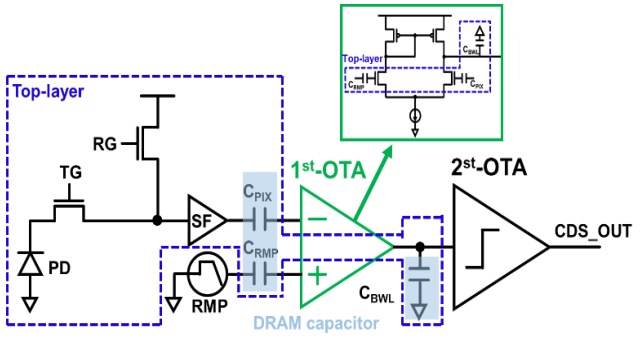
This paper has been verified using the transient-based AC simulation (TBAS) method [9] and demonstrated with the measurement results. The remainder of this paper is organized as follows. Section II describes the principle and architecture of the pixel-level SS ADC. Section III shows the simulation and measurement results with nBWL technique. Finally, the conclusion is given in Section IV.

II. Operational Principle and Architecture

A conceptual noise power spectral density (PSD) with/without BWL capacitor is shown in Fig. 1. In general, the temporal random noise (RN) of readout circuitry consists of two main components which are a flicker noise and a thermal noise in the frequency domain. Flicker noise is a low-frequency noise that has spectral density inversely proportional to the frequency. Flicker noise is caused by various sources such as amplifier's offset, kTC noise, and random fluctuations in the signals. By the correlated double sampling (CDS) function, the flicker noise in low-frequency is reduced and cancelled out. Thermal noise is mainly generated by the thermal motion of electrons in the transistor and it normally increase proportional to the circuit's bandwidth. Thus, a readout noise is finally decided by the both noise filters, the CDS function and -3dB cutoff frequency of comparator for SS ADC, as shown in Fig. 1. This paper describes the suppression of RN through the use of the BWL capacitor to shift lower band side for the -3dB cutoff frequency in the pixel-level ADC.



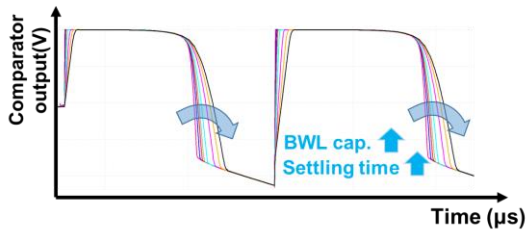
(a)



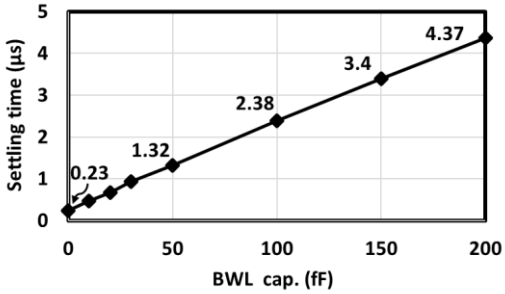
(b)

Figure 3. (a) Block diagram of the 2-stack structure and (b) Schematic of the pixel-level SS ADC.

The readout architectures of active pixel CMOS imagers are classified into three types as shown in Fig. 2, in largely where ADCs are located at columns and pixels. In Fig. 2(a), the readout architecture in rolling shutter, is commonly used in CMOS image sensors, performs A/D conversion start from the bottom of the sensor and top on the column ADC. Each row of pixels is exposed and readout sequentially, that creating a distortion effect on moving objects. The converted digital data is then sent out to the image signal processing (ISP). Fig. 2(b) shows



(a)



(b)

Figure 4. (a) Comparator output responses and (b) Signal settling time according to the capacitor's size of BWL.

the readout architecture in conventional global shutter. The exposure information, unlike rolling shutter CIS, is the same for 2-dimensional (2D) pixels and stored in-pixel memory with charge or voltage domain. This method eliminates the distortion effect in the rolling shutter. However, the readout method is exactly the same as rolling shutter CIS. In these method, the column ADC always operates during entire sensor operation. Therefore, the data conversion time is a key factor for the sensor speed in the column ADC architecture. On the other hand, the pixel-level ADC readout architecture performs analog-to-digital conversion on 2-dimensional pixel data in simultaneously as shown in Fig. 2(c). Then digitalized data is directly transfer ISP block. As a result, the ADC can have a sufficient time margin for the signal settle, and this architecture also can reduce the power consumption of each data converter. For the pixel-level SS ADC, even if it has the long term of A/D conversion period, sensor has no performance degradations such as a frame rate and noise. This means that the more aggressive nBWL technique can be used to the pixel-level readout circuitry for the noise suppression.

Fig. 3(a) and (b) show the block diagram of the developed 2-stack DPS structure and schematic of the pixel-level SS ADC, respectively. The prototype DPS is formed a 2-stack structure including photo-detector layer and analog/digital circuit layer. Top layer is composed of an active pixel sensor (APS) array with photo-diode and a part of the pixel-level SS ADC. Bottom layer consists of the rest of the pixel-level SS ADC array including in-pixel memory and the analog/digital circuits with a row driver (RDV) for the pixel signal control block, a vertical scanner (VSC) for choosing the pixel address number, a gray counter (GC),

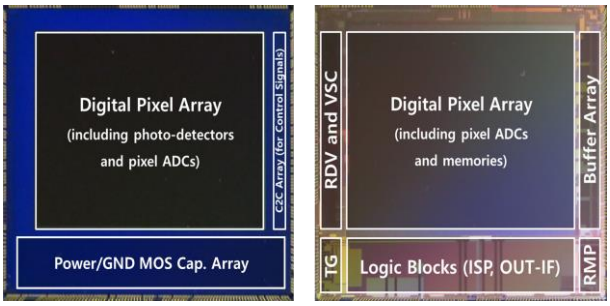


Figure 5. Chip micrographs (left: top chip, right: bottom chip).

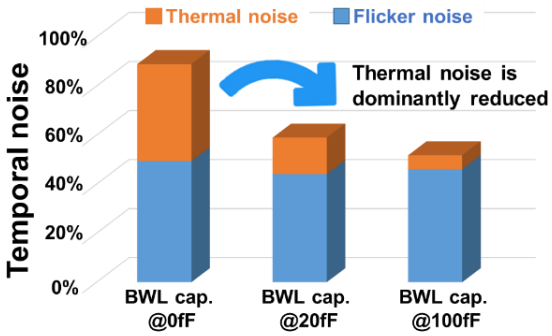
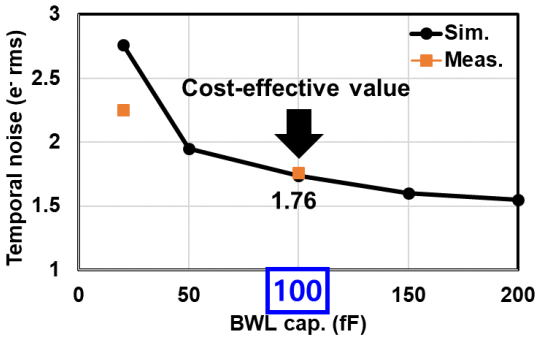


Figure 6. The simulated temporal noises of pixel-level SS ADC with the different BWL capacitors.

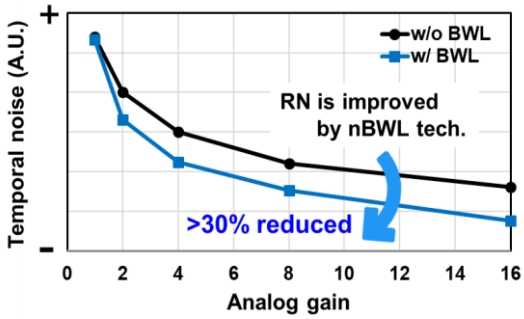
and a logic blocks for the image processing. Two layers including pixel-level ADCs have been bonded using Cu-to-Cu (C2C) process as shown in Fig. 3(a). Fig. 3(b) shows the simplified schematic of the pixel-level SS ADC. The input transistors of first-stage operational transconductance amplifier (OTA), the DRAM capacitors for AZ operation, and the DRAM capacitor for readout noise suppression using nBWL technique are implemented on the Top layer. A nBWL technique is one of the well-known noise suppression method for the readout circuit. However, depends on the size of BWL capacitor, the output settling time is gradually increased by increasing the output impedance. Fig. 4(a) and (b) show the output responses of comparator with different capacitor sizes and their settling times, respectively. At the capacitor size of 100fF, the total settling time of comparator output is expected around 4.8µs due to the reset and signal A/D conversions. A large settling time can limit the operation of image sensor.

III. Simultion and Measurement Results

A 2-Mp, 4.95-µm pixel pitch global shutter CMOS image sensor with pixel-level ADCs is implemented by using 65 nm (Top-layer with pixel part) and 28 nm (Bot-layer with logic part) CIS processes. The die micrographs of the top and bottom chips are shown in Fig. 5. The designed SS ADC has been verified using TBAS analysis method, and the sensor chip has been fully evaluated. The noise simulation results for demonstrating the



(a)



(b)

Figure 7. (a) The simulation and measurement results of sensor TN as a function of the capacitor's size for BWL (b) The measurement results of sensor TN as a function of the analog gain with and without BWL capacitor.

nBWL effect of pixel-level SS ADC are shown in Fig. 6. The thermal noise is sensitively decreased as a function of the BWL capacitor's size. As a result, a total RN is improved approximately over 30 % with the 100fF capacitor for nBWL. Fig. 7 shows the RN measurement results of fabricated DPS. The capacitor size of 100 fF is cost-effective value for pixel-level SS ADC with considering pixel pitch and sensor performances as can be seen from Fig. 7(a). Fig. 7(b) shows the measured noise trend with nBWL method as a function of analog gain. The measured RN of 1.76 e-rms is achieved with the 100fF BWL capacitor and the analog gain of 16 times. This result shows that the competitive low-noise pixel-level ADC can be realized, even if the comparator operates in sub-threshold region for the low-powered operation of the proposed readout architecture. The captured sample image is shown in Fig. 8. To analyze the RN trend with the nBWL technique, the top area of the image is assigned without BWL capacitor, and the right bottom and left bottom areas are assigned BWL capacitors of 100fF and 200fF, respectively. As can be seen from this sample image, the nBWL method is successfully worked and has been demonstrated without any image distortion.

IV. Conclusion

2-Mp GS-type with pixel-level ADC including RN reduction method has been presented and successfully

Figure 8. Captured sample image with BWL capacitor method.

demonstrated. We believe the pixel-level ADC will be a great alternative readout circuit solution to achieve the higher performance and functionality in the near future. The nBWL techniques with such readout chain are very effective method to improve the low-light performance of imager, especially digital pixel sensor (DPS) using pixel-level ADC.

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